AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs as indicated.

[0010] The present invention discloses a nonvolatile memory with spacer trapping structure, the nonvolatile memory comprising a semiconductor substrate; a gate oxide formed on the semiconductor substrate. A gate structure is formed on the gate oxide, wherein the gate structure comprises a stacked structure including polysilsicon layer/silicide layer and a first dielectric layer. A second dielectric layer is formed over the sidewall of the gate structure. First spacers are formed on the sidewall of the second dielectric layer for storing carrier and source and drain regions formed adjacent to the gate structure. And the p-n junctions of source and drain regions are located under the spacer structure.

[0045] Next, the embodiments shown in figure 17-24 are the alternative arrangements that are associated with figures 9-16, correspondingly. The main different is that the double-spacers structure is introduced into the embodiments shown in figure 17-24. The material for the first spacer 12 is oxide. The ONO structure is consisted of the oxide layer 10, nitride layer 11 and the oxide spacer 12. The second spacer 13 is attached on the first spacer 12, the second spacer can be formed of oxide, nitride or the material having energy gap larger than 4 eV. The configuration, therefore, constructs the double spacers structure.